

AMENDMENTS TO THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1.-22. (Canceled)

23. (Previously Presented) An embedded-DRAM (dynamic random access memory) processor comprising:

an embedded DRAM array comprising a plurality of random access memory cells arranged in rows and columns;

a row address register that holds a pointer that points to a row of the DRAM array; first and second registers files, each of said register files capable of loading or storing an entire row of the DRAM array in response to a single latch signal; and

an embedded processor comprising first and second functional units, said first and second functional units having respective first and second instruction sets and capable of accessing said first and second register files;

wherein said first and second register files comprise a parallel access port operative to parallelly transfer contents of one of said register files between a DRAM row as selected by said row-address register, said first and second register files further comprising at least a second access port operative to transfer data between a selected one of said register files and said second functional unit;

wherein said first instruction set comprises at least:

(i) a command to manipulate data in a data register within a register file; and

wherein said second instruction set comprises at least:

(ii) a command to perform an arithmetic operation on said row address register;

(iii) a command to load the entire row pointed to by said row address register into a selected set of registers of said register files in a single operation.

24. (Previously Presented) The embedded-DRAM processor according to Claim 23, wherein said first and second functional units each respectively execute a command from said first and second instruction sets substantially contemporaneously.

25. (Previously Presented) The embedded-DRAM processor according to Claim 24, further comprising:

a first software module comprising data manipulation commands drawn from said first instruction set, said first software module executed by said first functional unit; and

a second software module comprising a parallel data transfer command drawn from said second instruction set, said second software module being executed by said second functional unit;

whereby said second software module operates in support of said first software module to prefetch data from said DRAM array into one of said register files in advance of said data being needed by said first software module.

26. (Previously Presented) The embedded-DRAM processor of Claim 23, wherein the second instruction set further comprises

(iv) a command to toggle a register set between an active state and an inactive state.

27. (Previously Presented) The embedded-DRAM processor of Claim 26, wherein said toggle command causes said first register file to toggle from the inactive state to the active state and also causes the second register file to toggle from the active state to the inactive state.

28.-49. (Canceled)

50. (Previously Presented) An embedded-DRAM (dynamic random access memory) processor comprising:

an embedded DRAM array comprising a plurality of random access memory cells arranged in rows and columns;

an embedded row address register that holds a pointer that points to a row of the embedded DRAM array;

embedded first and second registers files, each of said register files capable of loading or storing an entire row of the DRAM array in response to a single latch signal, each of said register files also being capable of being placed into an active state and an inactive state; and

embedded first and second of functional units, said first and second functional units having respective first and second instruction sets and capable of accessing said first and second register files while in said active state;

wherein said first and second registers files comprise a parallel access port operative to parallelly transfer contents of said register file between a DRAM row as selected by said row-address register, each of said register file further comprising at least a second access port operative to transfer data between a selected register file and said second functional unit;

wherein said first instruction set comprises at least:

a command to manipulate data in a data register within a register file; and wherein said second instruction set comprises at least:

a command to perform an arithmetic operation on said row address register; and

a command to load the entire row pointed to by said row address register into a selected set of registers of said register files that is currently in the inactive state, wherein loading the entire row is performed in a single operation.

51. (Canceled)